DESIGN AND DEVELOPMENT OF CODE AND CARRIER TRACKING ALGORITHM IN CDMA SYSTEMS

CHANDU SAI REVATHI[#] , N. RENUKA[##]

#COMMUNICATION AND SIGNAL PROCESSING, M.TECH

##ASSOCIATE PROFESSOR, ECE DEPARTMENT

RVR AND JCCE COLLEGE OF ENGINEERING, GUNTUR, A.P, INDIA

saiechandu@gmail.com, ravirenu_v@yahoo.co.in

ABSTRACT:

In digital communication systems, the need of using multiple access techniques is predominant as number of users is increasing day by day. In case of communication systems, which gives more importance to saving the bandwidth and secrecy of information, the CDMA (Code Division Multiple Access) technology is best among TDMA, FDMA and CDMA. CDMA multiple access technique makes the system to transmit/receive information at all time throughout the frequency. In CDMA technique, each user is assigned a unique code to avoid interference. These codes are chosen so that they are orthogonal to each other. Here, the data sequence is multiplied with the code sequence which results a spreading sequence thus CDMA is called spread spectrum technique. The spreading sequence hides the data which enables privacy and other advantages are interference suppression, energy density reduction and it is used for delay measurement. In this paper, the spreading is done using direct sequence spread spectrum technique.

The receiver has to acquire the data that is given at the transmitter; this involves acquisition, code tracking, demodulation (carrier tracking) and bit synchronization. Integrated code and carrier tracking loop is combination of code tracking and demodulation. This integrated loop in receiver makes system less hardware and faster than conventional receiver because code tracking and demodulation work in parallel in integrated loop. The receiver of the system will have acquisition, integrated code and carrier tracking loop and bit synchronization.

Keywords: CDMA, Non Coherent, Code Tracking, Carrier Tracking, Integrated loop.

I. INTRODUCTION

In digital communication systems, by using CDMA technique we can achieve secrecy and anti jamming. This also reduces the frequency usage. In CDMA, each user is distinguished by PN (Pseudo random Noise) code. The data/information is spread over the PN sequence thus CDMA is called Spread Spectrum technique. Since data hides in PN code, it helps in maintaining the secrecy [1]. The spread data is modulated using Direct Sequence Spread Spectrum modulation technique. The conventional receiver block diagram is shown in figure1. The integrated loop block diagram is shown in figure2. This paper mainly focuses on fine synchronization of code and carrier frequencies. In integrated loop, prompt, early and late data of both in-phase and Quadrature phase are processed for fine synchronization. Early and late data is calculated by taking ½ bit chip difference. In-phase and Quadrature phase are related to carrier signal and early, prompt and late are related to locally generated PN code at the receiver.

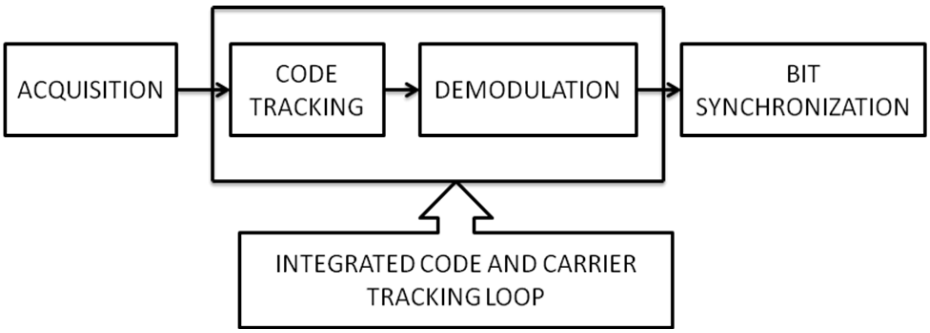

Fig.1 Conventional Receiver Block Diagram

The integrated loop consists of two parts: code tracking loop and carrier tracking loop. Code tracking loop is performed using DLL (Delay Lock Loop) algorithm. Carrier tracking loop is performed using FLL and PLL [3]. FLL (Frequency Lock Loop) function is to track the frequency when large Doppler shifts in carrier present. A minimum power level is required for working of PLL (Phase Lock Loop). FLL helps in increasing the power of the received signal. So, in carrier tracking loop FLL works for a particular time and then PLL starts working after that. GPS specifications are used for simulation purpose.

The paper is organised as follows: in section 2, DLL algorithm is explained, in section 3, FLL and PLL algorithms are explained. Section 4 presents simulation results. Conclusion is presented in section 5.

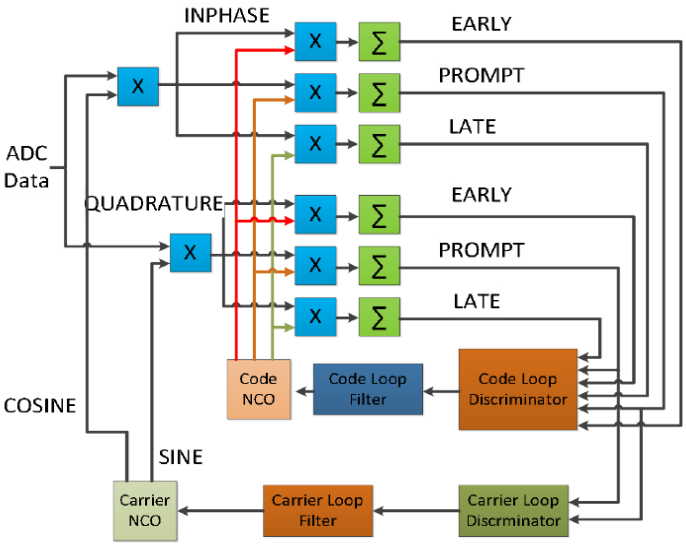

Fig.2 Integrated Code and Carrier Tracking Loop

II. CODE TRACKING ALGORITHM

The Code Tracking algorithm presented in this paper Non-Coherent Delay Lock Loop (DLL), which uses early, late and prompt gates that we can observe in Fig.2. The correlations values of early, late and prompt are calculated by using integrate and dump circuits. The integration time is code phase time period. These are denoted as I_E, Q_E, I_L, Q_L, I_P and Q_P, where I and Q represent In-phase and Quadrature phase. The DLL has code loop discriminator, code loop filter and code NCO. The code loop discriminator process the code error. The code loop filter used to make the system stable even though there are frequent changes in the error. Here, code loop filter used is second order filter [2]. Code NCO (Numerically Controlled Oscillator) function is to generate the code frequency that varies with code error.

A. Code loop discriminator:

The code loop discriminator used is quasi coherent discriminator and is given by

$$e(t) = (I_E * I_E) + (Q_E * Q_E) - (I_L * I_L) + (Q_L * Q_L)$$

The advantage of this discriminator is its performance is effective even in the presence of noise in the system.
This discriminator is normalized using the equation given below:

III. CARRIER TRACKING ALGORITHM

The Carrier Tracking algorithm consists of FLL and PLL [4]. FLL is used to track the frequency of large Doppler. PLL tracks the phase of the carrier. He carrier tracking blocks can be observed in the Fig.2. The All paragraphs must be indented. The carrier discriminators are discussed in the following section. The loop filters are second order loop filters. Carrier NCO output gives the frequency of the carrier in accordance with the error feeding it.

A. Carrier Tracking Discriminators:

The discriminator used for FLL is given as:

$$e(t) = I_P^t * Q_P^{t-1} - I_P^{t-1} * Q_P^t$$

Where, I_P^t and Q_P^t are in-phase and Quadrature phase prompt values at time t.

I_P^{t-1} and Q_P^{t-1} are in-phase and Quadrature phase prompt values at time t-1.

The discriminator used for PLL is given as:

$$e(t) = I_P^t * Q_P^t$$

IV. SIMULATION RESULTS

The simulation is done using VHDL coding. In Fig.3, the Doppler of 6 Hz for code and 250Hz for carrier is taken for simulation purpose. Simulation is done by taking 12 different users having differentiated by PN codes. Once the code and carrier frequencies are tracked data comes in I arm. Now the data is synchronized with data clock using bit synchronizer.

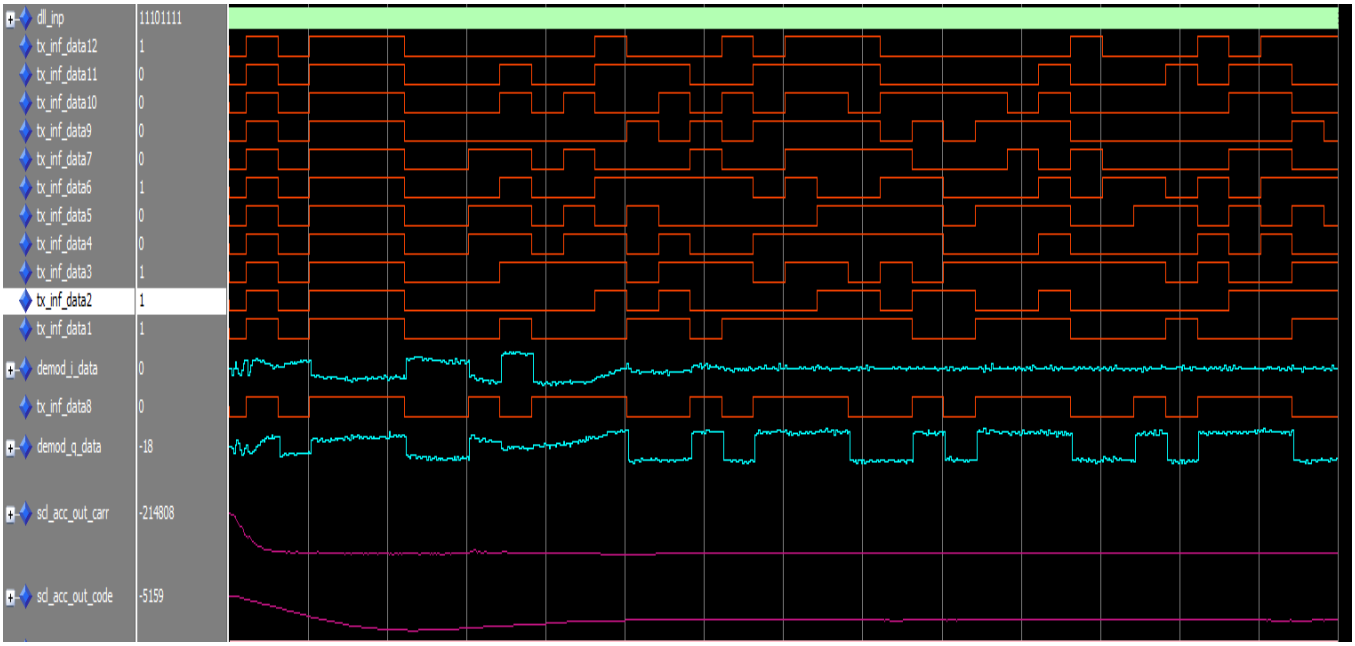

Fig.3. Simulation Result of Tracking Loop

In this simulation data is observed in user 8. In another case data is observed in user 12. This is shown in Fig.4.

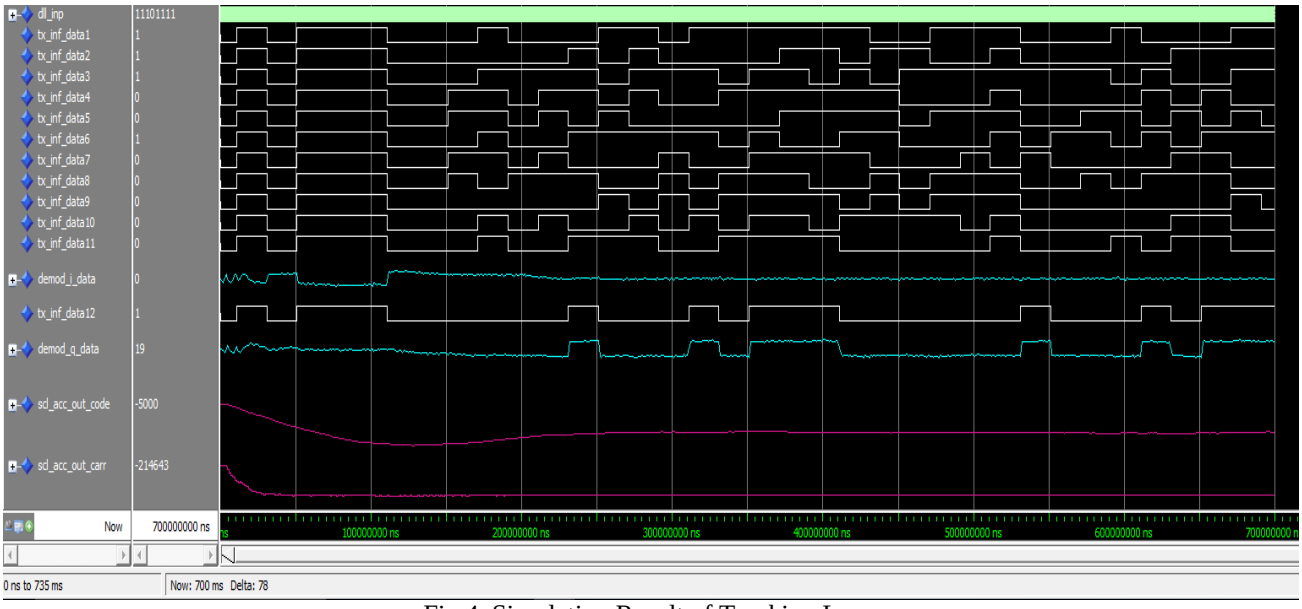

Fig.4. Simulation Result of Tracking Loop

V. CONCLUSION

In CDMA systems, using integrated racking loop in the Tracking system has the following advantages:

- Hardware usage in FPGA is less when compared with band pass filter version type of code tracking.
- Processing time is less, so this tracking loop makes the system faster.

- It withstands noise in the system and can do the fine synchronization.

The only disadvantage in this system is it does not work for third order loop filter in the system.

REFERENCES

[1] *E. D. Kaplan and C. J. Hegarty, Understanding GPS, Principles and Applications, 2nd Edition, Norwood, MA: Artech House, Inc., 2006.*
[2] *JAMES BAO-YEN TSUI, Fundamentals of Global Positioning System receivers.*
[3] *REAL-TIME SOFTWARE DEFINED GPS RECEIVER, a thesis submitted to the Faculty of Purdue University by Jeremy Hershberger, August 2013, Purdue University, Fort Wayne, Indiana.*
[4] *A software- Defined GPS and Galileo Receiver, A single frequency Approach by Kai Borre, Dnnis M.Akos, Nicolaj Bertelsen, Peter Rinder, Soren Holdt Jensen.*